☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: V460H1
SUFFIX: LH5

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Josh Chi	Lynn Cheng

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.1	Jan. 21, 2011	All	All	The Approval Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V460H1-LH5 is a 46" TFT Liquid Crystal Display module with 16-CCFL Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 1.073G colors (8-bit+FRC). The balance board module for backlight is built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (5000:1)
- Fast response time (Gray to gray average 4.5 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- RoHs compliance

1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1018.08(H) x 572.67 (V) (46" diagonal)	mm	(1)
Bezel Opening Area	1024.4 (H) x 578.6 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.17675 (H) x 0.53025 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.073G	color	-
Display Operation Mode	Transmissive mode / Normally Black	-	-
Surface Treatment	Glare coating (super clear), Hardness (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	-	1083.0	-	mm	(1)
	Vertical (V)	-	627.0	-	mm	(1)
	Depth (D)	-	53.2	-	mm	(2)
Weight		-	13213	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to balance board cover.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	50.0	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

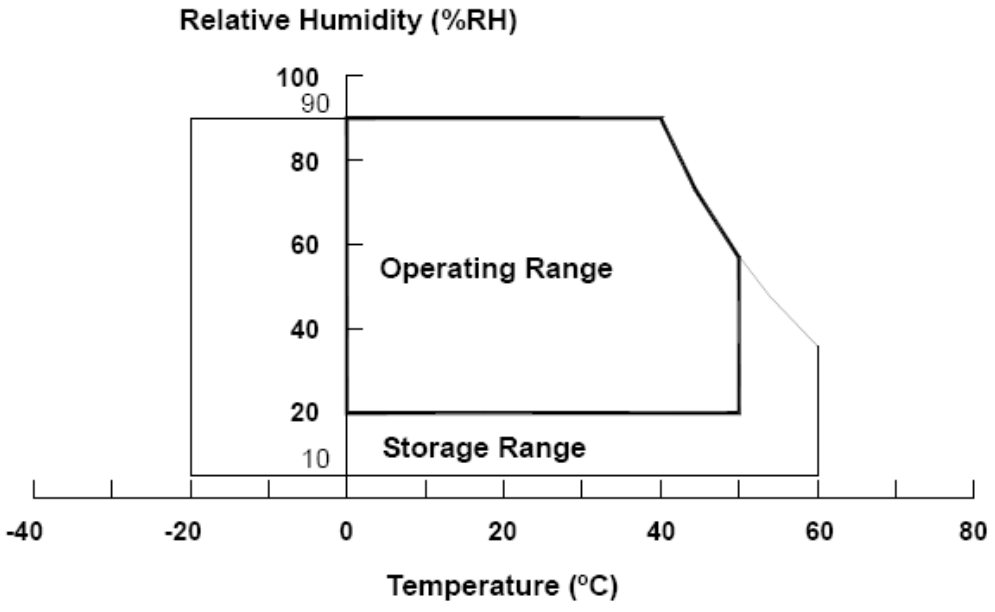
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT BALANCE BOARD UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V	-	3000	VRMS	Lamp Voltage

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

3. ELECTRICAL CHARACTERISTICS

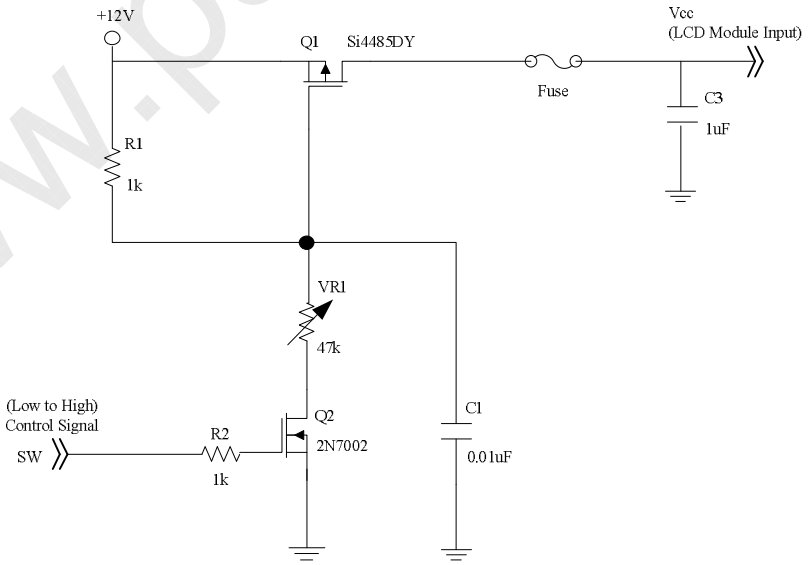
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

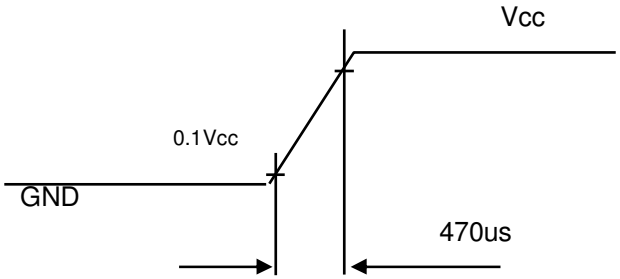
Parameter			Symbol	Value			Unit	Note
				Min.	Typ.	Max.		
Power Supply Voltage			V_{CC}	10.8	12	13.2	V	(1)
Rush Current			I_{RUSH}	-	-	4.4	A	(2)
Power Supply Current		White Pattern		-	1.1	1.45	A	(3)
		Black Pattern		-	0.95			
		Horizontal Stripe		-	1.9	2.47		
LVDS interface	Differential Input High Threshold Voltage		V_{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage		V_{LVTL}	-	-	-100	mV	
	Common Input Voltage		V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)		$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor		R_T	-	100	-	ohm	
CMIS interface	Input High Threshold Voltage		V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage		V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement Conditions:

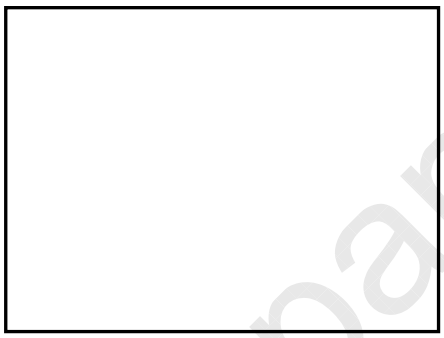


Vcc rising time is 470us



Note (3) The specified power supply current and power consumption is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

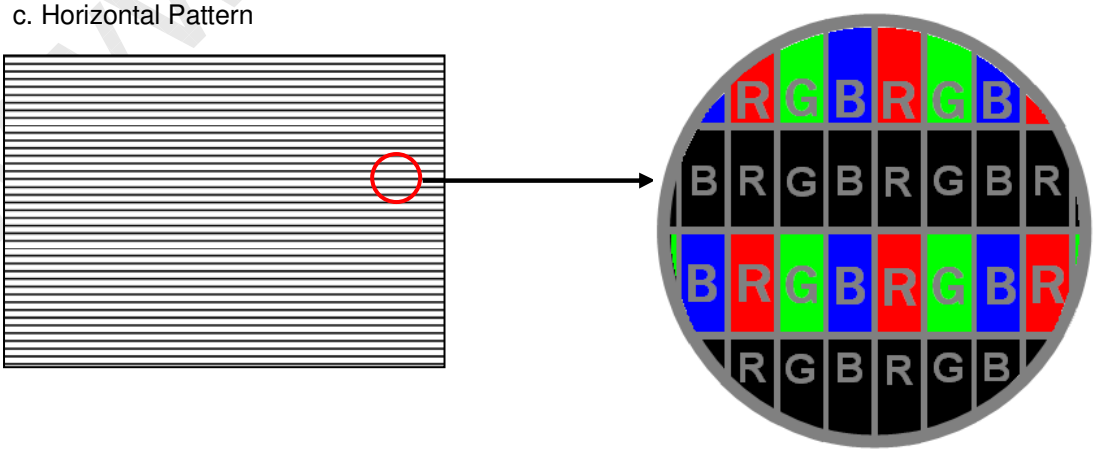


Active Area

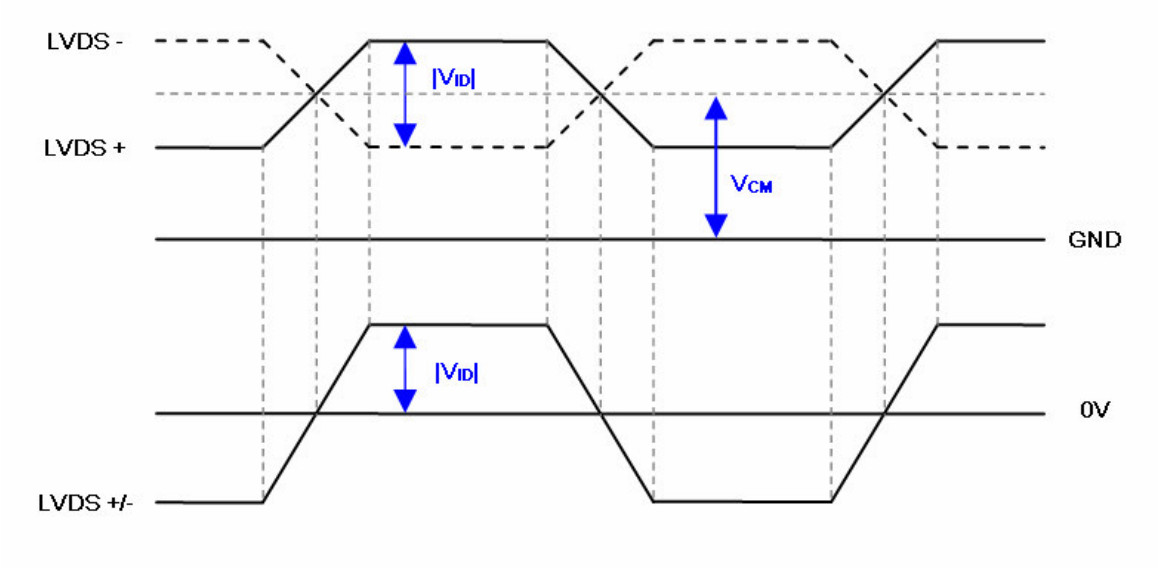
b. Black Pattern

Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LAMP SPECIFICATION (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1170	-	V_{RMS}	-
Lamp Current	I_L	10.2	10.5	10.8	mA_{RMS}	
Lamp Turn On Voltage	V_S	-	-	2050	V_{RMS}	(1) , Ta = 0 ºC
		-	-	1660	V_{RMS}	(1) , Ta = 25 ºC
Operating Frequency	F_O	30	-	80	KHz	(2)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(3)

3.2.2 ELECTRICAL SPECIFICATION (Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Input High Voltage		High	-	1180	-	Vrms	(6)
Protection Circuit Supply Voltage		Vcc	10	12	15	V	
Input Current		$I_{BL(HV)}$		175		mArms	
Oscillating Frequency		F_W	43	46	49	kHz	
Individual Lamp Current		I_L	10.2	10.5	10.8	mA	(5)
Lamp Detection	High	LD	5	-	-	V	Normal Operation
	Low	LD	-	-	1.5	V	Lamp Connector Open
Dimming frequency		F_B	135	150	165	Hz	
Minimum Duty Ratio		D_{MIN}		15		%	(8)

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.:

Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

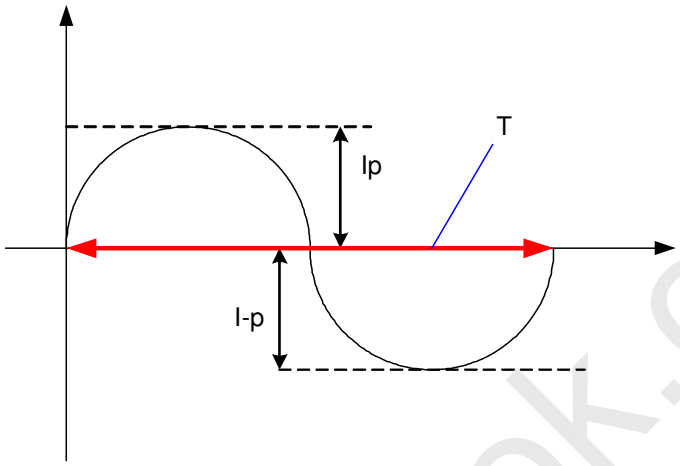
Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 11~13mArms.

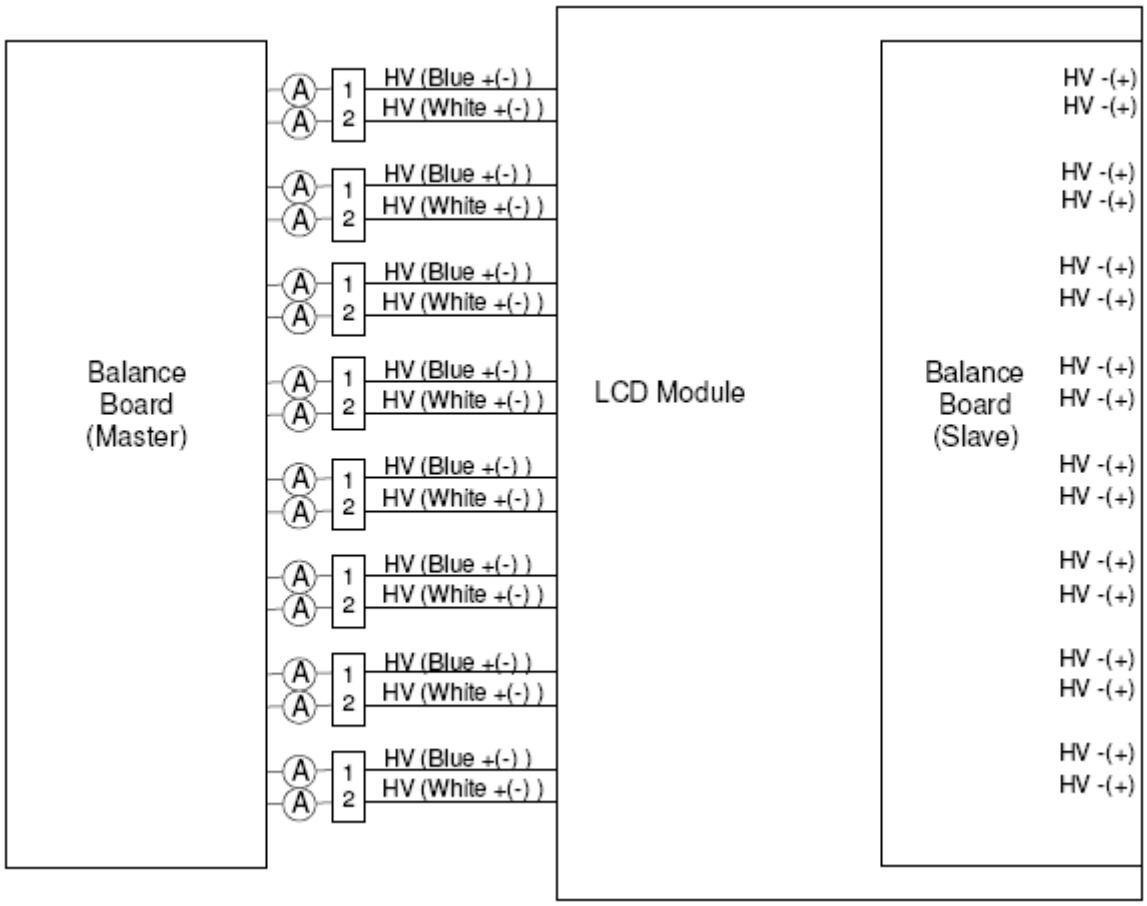
Note (5) Lamp current is measured master board by utilizing high frequency current meters as shown below:

Note (6) Input voltage Hv based on spec. +-7% tolerance.

Note (7) Asymmetric ratio must be from 90% to 110% ($0.9<Ip/ I_{rms@T/2X\sqrt{2}}<1.1$)

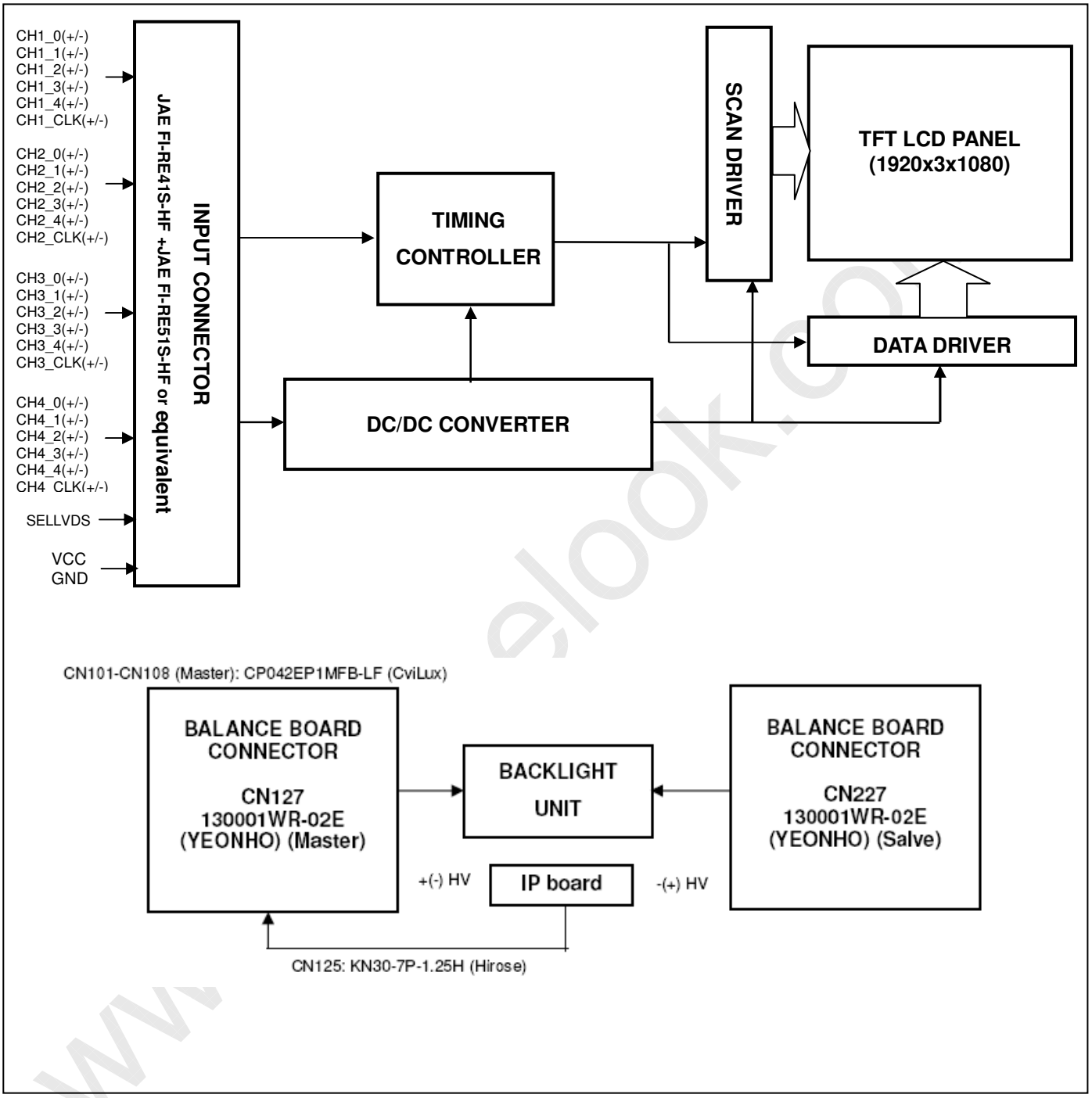
Note (8) The minimum dimming under 7% operation should cause shutdown by protection circuit.





4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF3 Connector Pin Assignment (FI-RE41S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	
10	CH3_0N	Third Pixel Negative LVDS differential data input. Channel 0	(4)
11	CH3_0P	Third Pixel Positive LVDS differential data input. Channel 0	
12	CH3_1N	Third Pixel Negative LVDS differential data input. Channel 1	
13	CH3_1P	Third Pixel Positive LVDS differential data input. Channel 1	
14	CH3_2N	Third Pixel Negative LVDS differential data input. Channel 2	
15	CH3_2P	Third Pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	CH3_CLKN	Third Pixel Negative LVDS differential clock input.	
18	CH3_CLKP	Third Pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3_3N	Third Pixel Negative LVDS differential data input. Channel 3	(4)
21	CH3_3P	Third Pixel Positive LVDS differential data input. Channel 3	
22	CH3_4N	Third Pixel Negative LVDS differential data input. Channel 4	
23	CH3_4P	Third Pixel Positive LVDS differential data input. Channel 4	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	
26	CH4_0N	Fourth Pixel Negative LVDS differential data input. Channel 0	(4)
27	CH4_0P	Fourth Pixel Positive LVDS differential data input. Channel 0	
28	CH4_1N	Fourth Pixel Negative LVDS differential data input. Channel 1	
29	CH4_1P	Fourth Pixel Positive LVDS differential data input. Channel 1	
30	CH4_2N	Fourth Pixel Negative LVDS differential data input. Channel 2	
31	CH4_2P	Fourth Pixel Positive LVDS differential data input. Channel 2	
32	GND	Ground	
33	CH4_CLKN	Fourth Pixel Negative LVDS differential clock input.	
34	CH4_CLKP	Fourth Pixel Positive LVDS differential clock input.	
35	GND	Ground	(4)
36	CH4_3N	Fourth Pixel Negative LVDS differential data input. Channel 3	
37	CH4_3P	Fourth Pixel Positive LVDS differential data input. Channel 3	
38	CH4_4N	Fourth Pixel Negative LVDS differential data input. Channel 4	
39	CH4_4P	Fourth Pixel Positive LVDS differential data input. Channel 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	

CNF2 Connector Pin Assignment (FI-RE51S-HF-J(JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(2)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	CH1_0N	First Pixel Negative LVDS differential data input. Channel 0	(3)
13	CH1_0P	First Pixel Positive LVDS differential data input. Channel 0	
14	CH1_1N	First Pixel Negative LVDS differential data input. Channel 1	
15	CH1_1P	First Pixel Positive LVDS differential data input. Channel 1	
16	CH1_2N	First Pixel Negative LVDS differential data input. Channel 2	
17	CH1_2P	First Pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	CH1_CLKN	First Pixel Negative LVDS differential clock input.	
20	CH1_CLKP	First Pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1_3N	First Pixel Negative LVDS differential data input. Channel 3	(3)
23	CH1_3P	First Pixel Positive LVDS differential data input. Channel 3	
24	CH1_4N	First Pixel Negative LVDS differential data input. Channel 4	
25	CH1_4P	First Pixel Positive LVDS differential data input. Channel 4	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	
28	CH2_0N	Second Pixel Negative LVDS differential data input. Channel 0	(3)
29	CH2_0P	Second Pixel Positive LVDS differential data input. Channel 0	
30	CH2_1N	Second Pixel Negative LVDS differential data input. Channel 1	
31	CH2_1P	Second Pixel Positive LVDS differential data input. Channel 1	
32	CH2_2N	Second Pixel Negative LVDS differential data input. Channel 2	
33	CH2_2P	Second Pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	CH2_CLKN	Second Pixel Negative LVDS differential clock input.	
36	CH2_CLKP	Second Pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2_3N	Second Pixel Negative LVDS differential data input. Channel 3	(3)
39	CH2_3P	Second Pixel Positive LVDS differential data input. Channel 3	
40	CH2_4N	Second Pixel Negative LVDS differential data input. Channel 4	
41	CH2_4P	Second Pixel Positive LVDS differential data input. Channel 4	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	

46	GND	Ground	
47	N.C.	No Connection	
48	Vin	Power input (+12V)	
49	Vin	Power input (+12V)	
50	Vin	Power input (+12V)	
51	Vin	Power input (+12V)	

Note (1) Please be reserved to open.

Note (2) Low or Open: VESA Format(default), connect to GND. High: JEIDA Format, connect to+3.3V.

Note (3) LVDS 4-Port Data Mapping

Port	CH of LVDS	Data Stream
1st Port	First pixel	1, 5, 9, ..., 1913, 1917
2nd Port	Second pixel	2, 6, 10, ..., 1914, 1918
3rd Port	Third pixel	3, 7, 11, ..., 1915, 1919
4th Port	Fourth pixel	4, 8, 12, ..., 1916, 1920

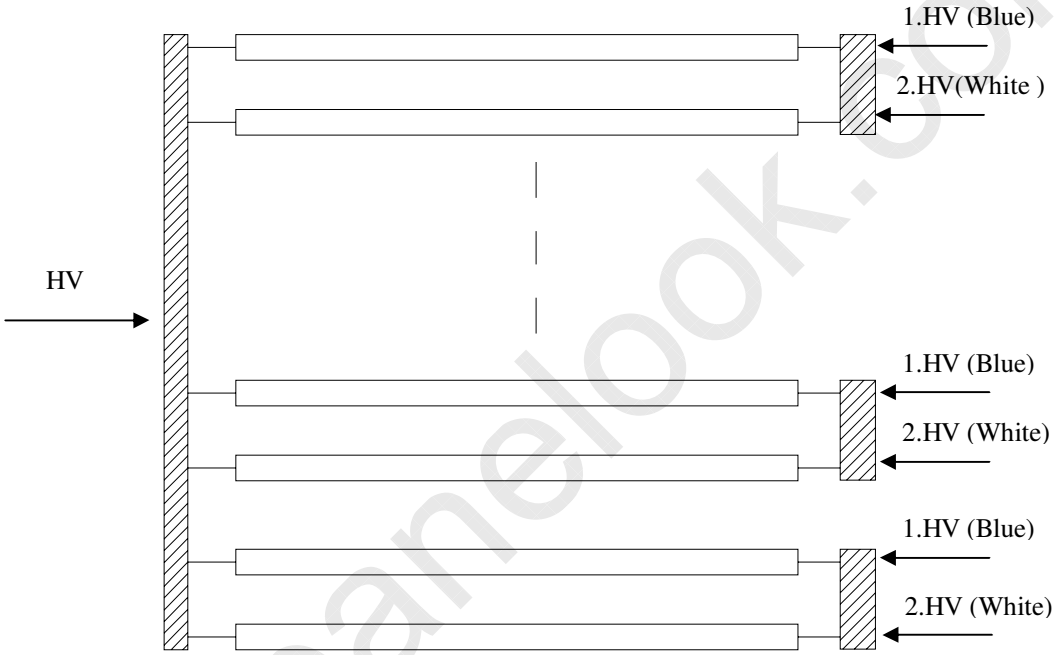
5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN101-CN108: CP042ESFA00 (Cvilux)

Pin	Name	Description	Wire Color
1	HV	High Voltage	Blue
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model CP042ESFA00, manufactured by Cvilux. The mating header on inverter part number is CP042EP1MFB-LF (Cvilux)



5.3 BALANCE BOARD UNIT

CN127 (Header) (Master): 130001WR-02E (YEONHO)

Pin No.	Symbol	Description
1	HV+(-)	High Voltage Input
2	HV+(-)	High Voltage Input

CN227 (Header) (Slave): 130001WR-02E (YEONHO)

Pin No.	Symbol	Description
1	HV-(+)	High Voltage Input
2	HV-(+)	High Voltage Input

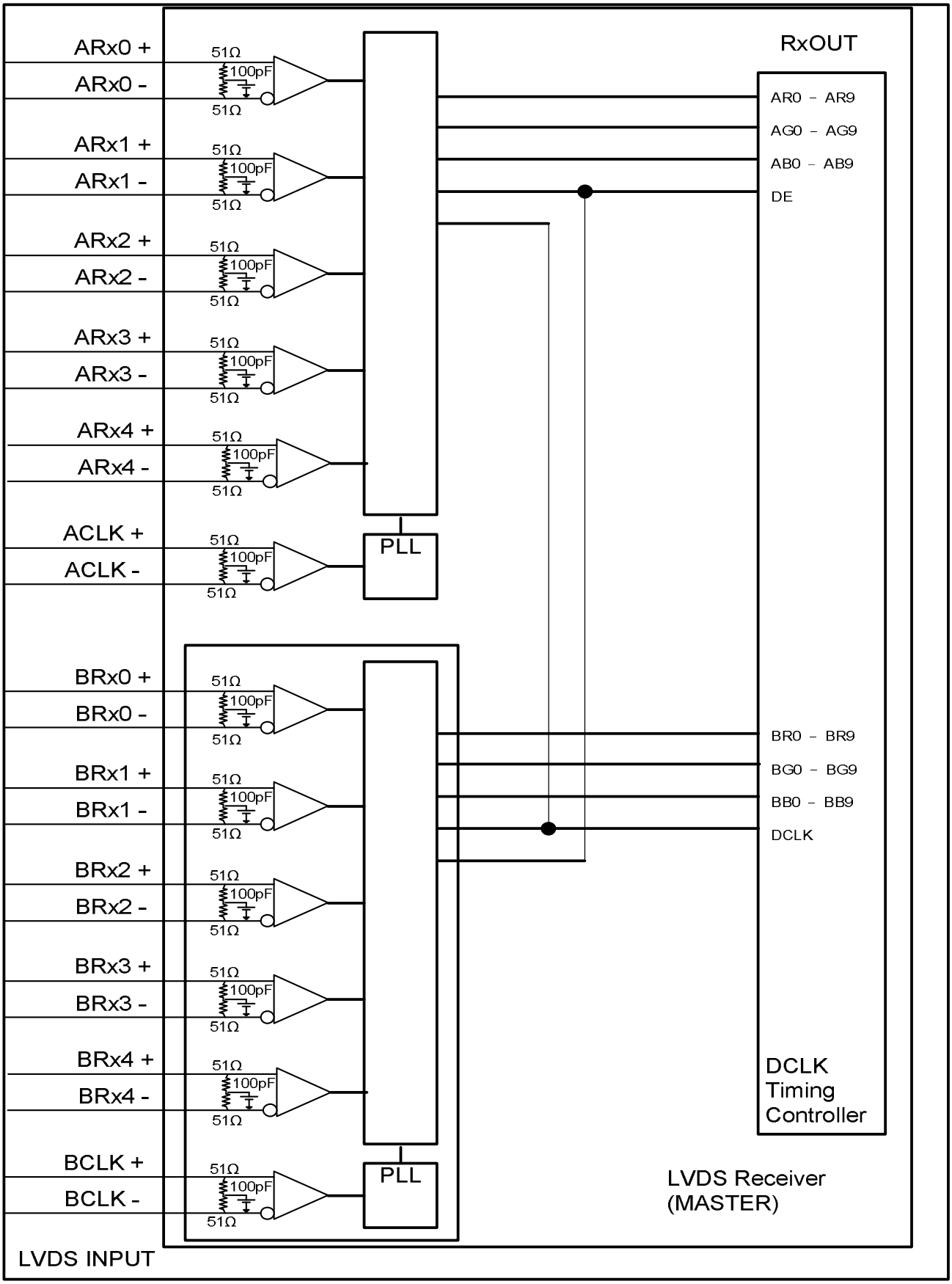
CN101-CN108 (Header) (Master): CP042EP1MFB-LF (CviLux)

Pin No.	Symbol	Description
1	CCFL HOT	CCFL High voltage
2	CCFL HOT	CCFL High voltage

CN125 (Header): KN30-7P-1.25H (Hirose).

Pin No.	Symbol	Description
1	VCC	Power Supply for Protection Circuit
2	FB1	Lamp Current Feedback 1
3	FB2	Lamp Current Feedback 2
4	GND	Signal Ground
5	GND	Signal Ground
6	LD	CCFL Connector Open & Non-lighting signal
7	LD	CCFL Connector Open & Non-lighting signal

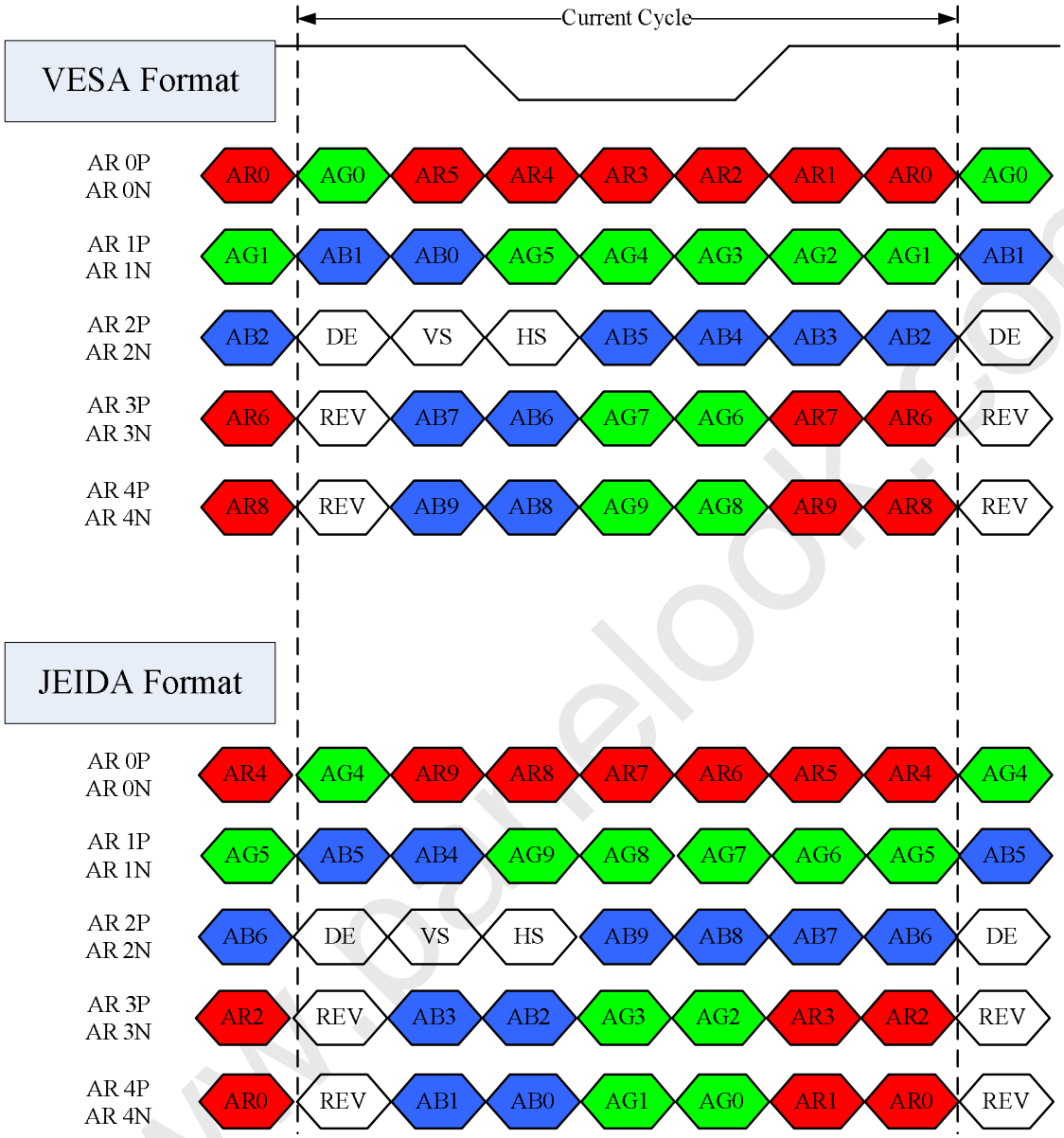
5.4 BLOCK DIAGRAM OF INTERFACE



5.5 LVDS INTERFACE

VESA Format: SELLVDS = H or Open

JEIDA Format: SELLVDS = L



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	-	100	-	Hz	
		F_{r6}	-	120	-	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	
	Blank	Tvb	35	45	55	Th	
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	
	Blank	Thb	60	70	95	Tc	

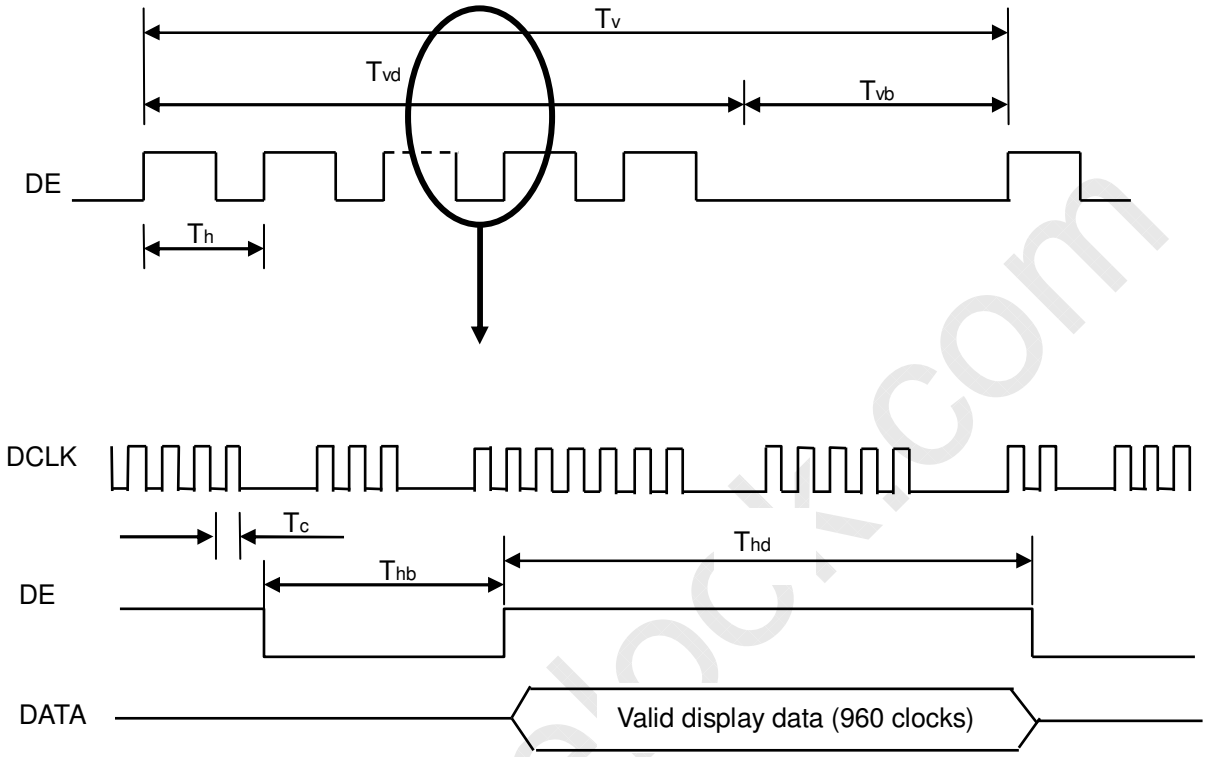
Note (1) Please make sure the range of pixel clock has follow the below equation :

Fclkin(max) ≧ Fr6 × Tv × Th

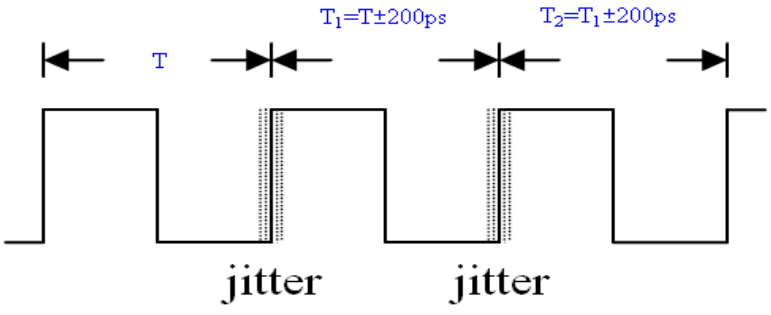
Fr5 × Tv × Th ≧ Fclkin(min)

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

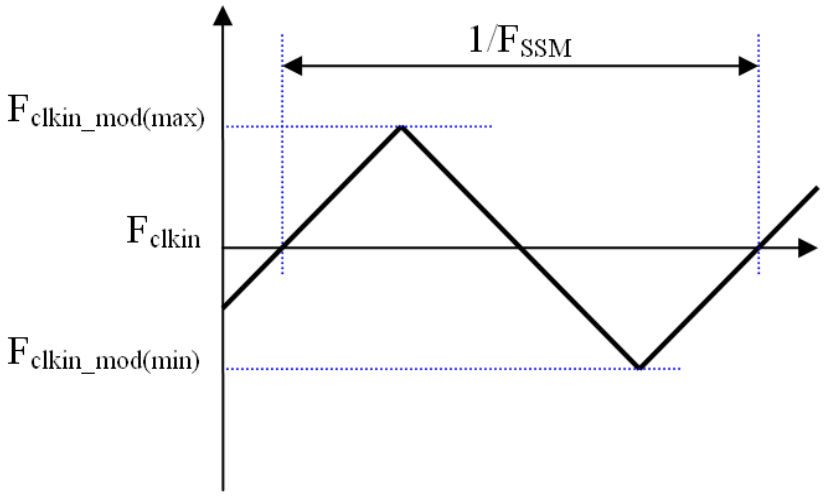
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

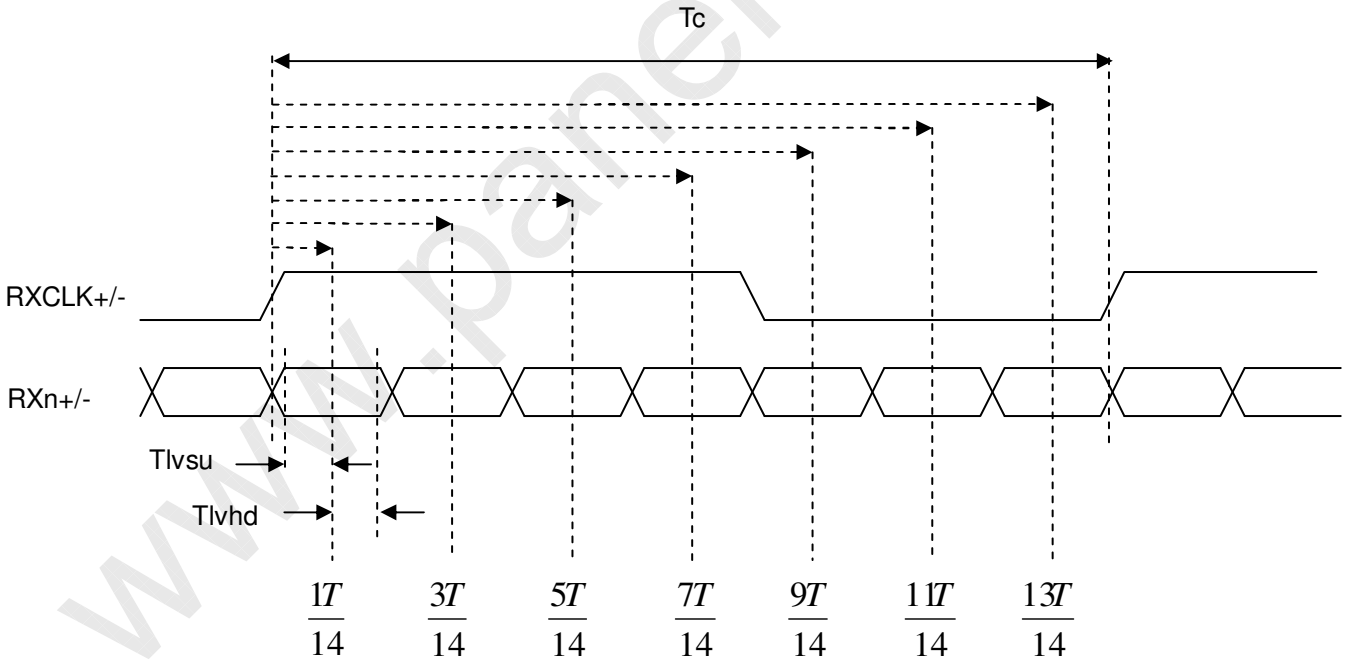


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

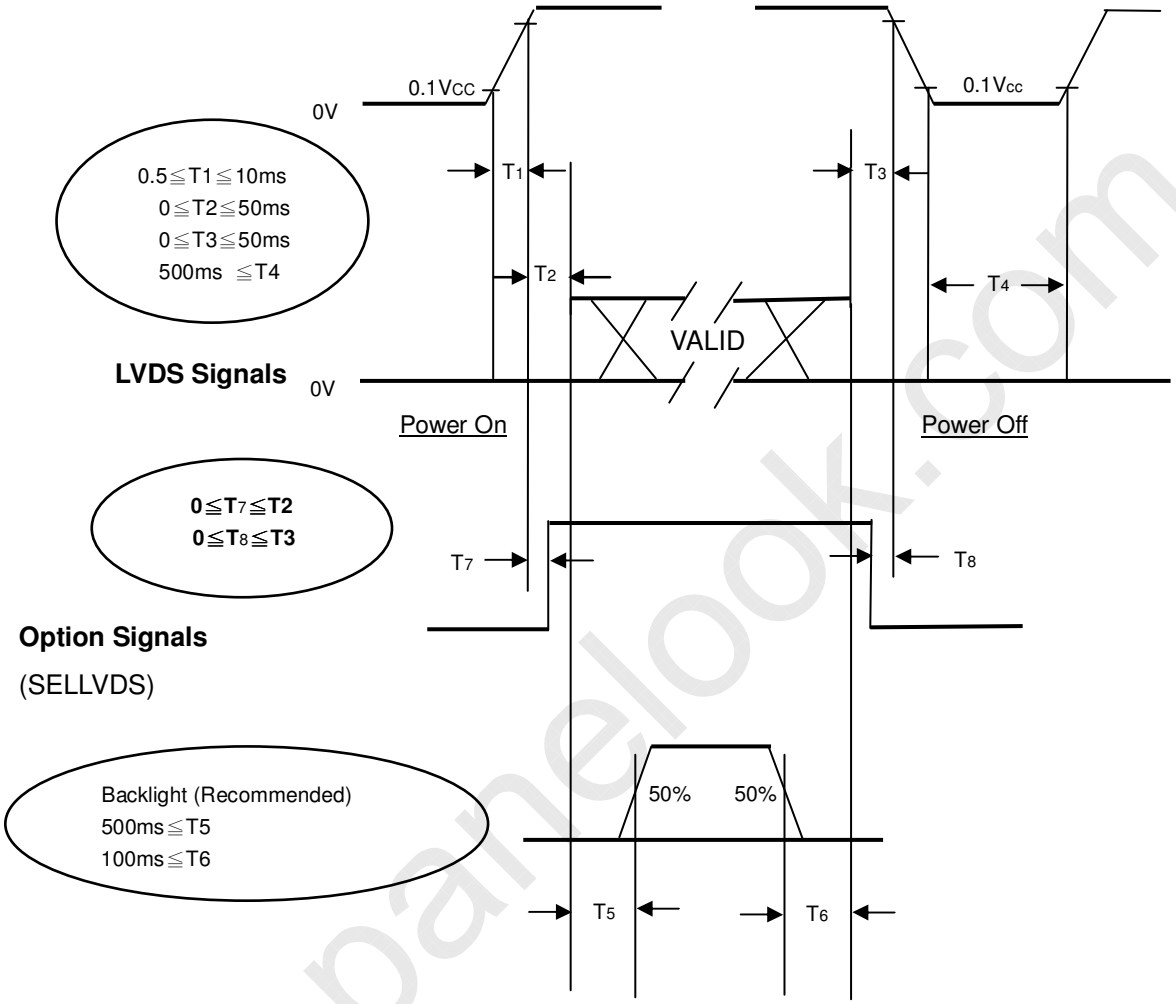
LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

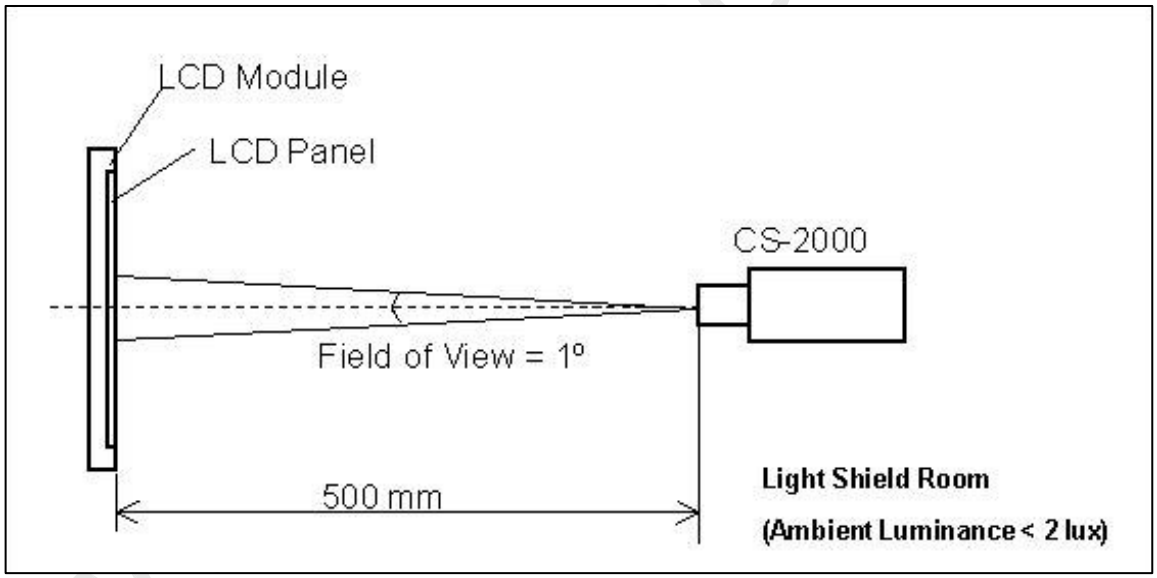
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	10.5±0.3	mA
Oscillating Frequency (Inverter)	FW	46±3	KHz
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



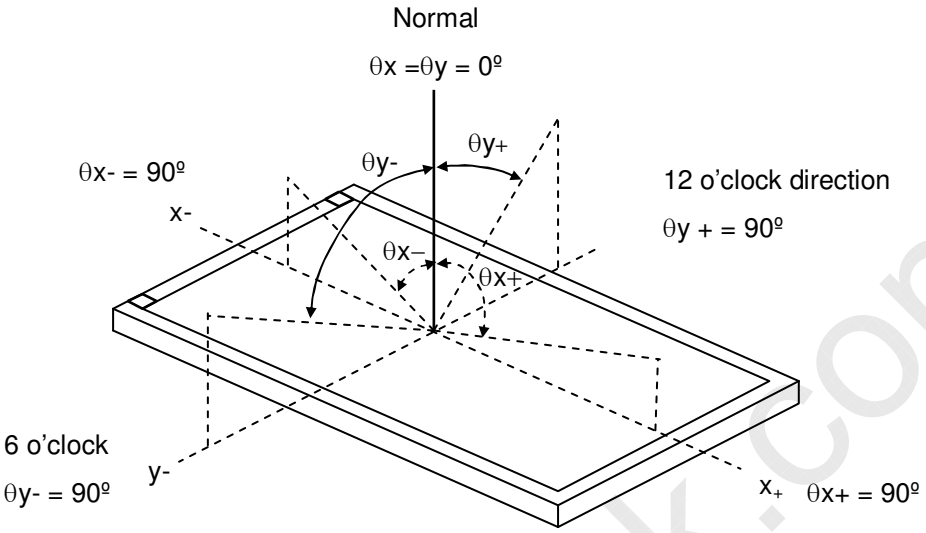
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	4000	5000	-	-	(2)
Response Time (VA)		Gray to gray		-	4.5	8	ms	(3)
Center Luminance of White		L_C		400	500	-	cd/m^2	(4)
White Variation		δW		-	-	1.3	-	(6)
Cross Talk		CT		-	-	4	%	(5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.634	Typ. +0.03	-	-
		Ry			0.323		-	
	Green	Gx			0.287		-	
		Gy			0.602		-	
	Blue	Bx			0.148		-	
		By			0.056		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Color Gamut	C.G		-	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.	(1)
		θx-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

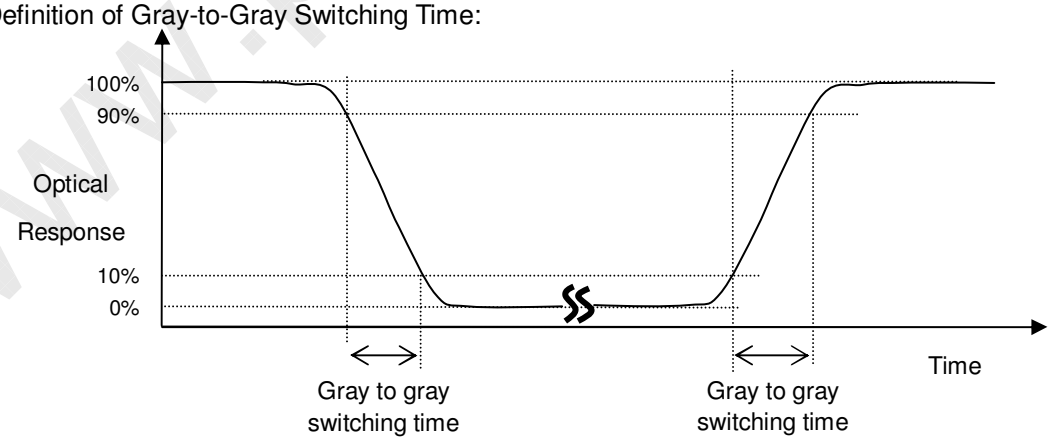
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

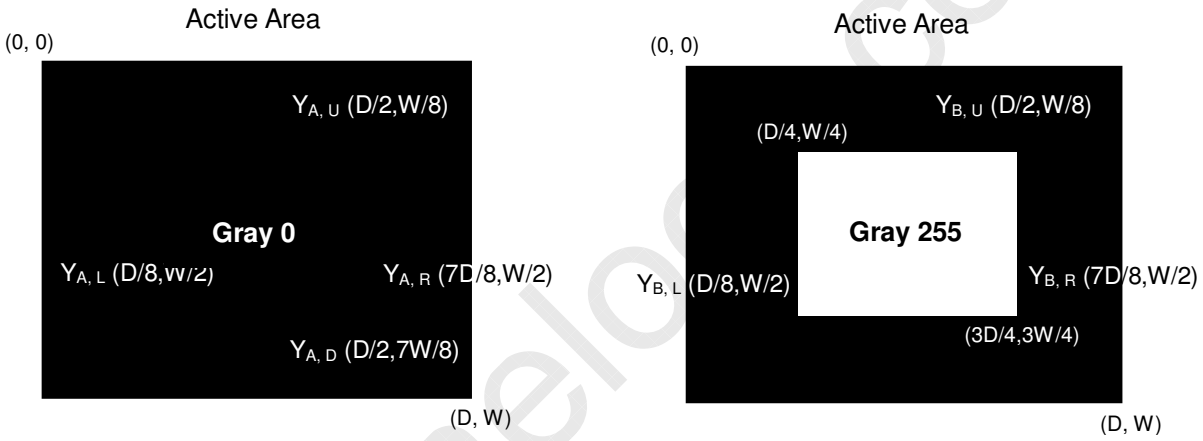
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 255 pattern (cd/m2)

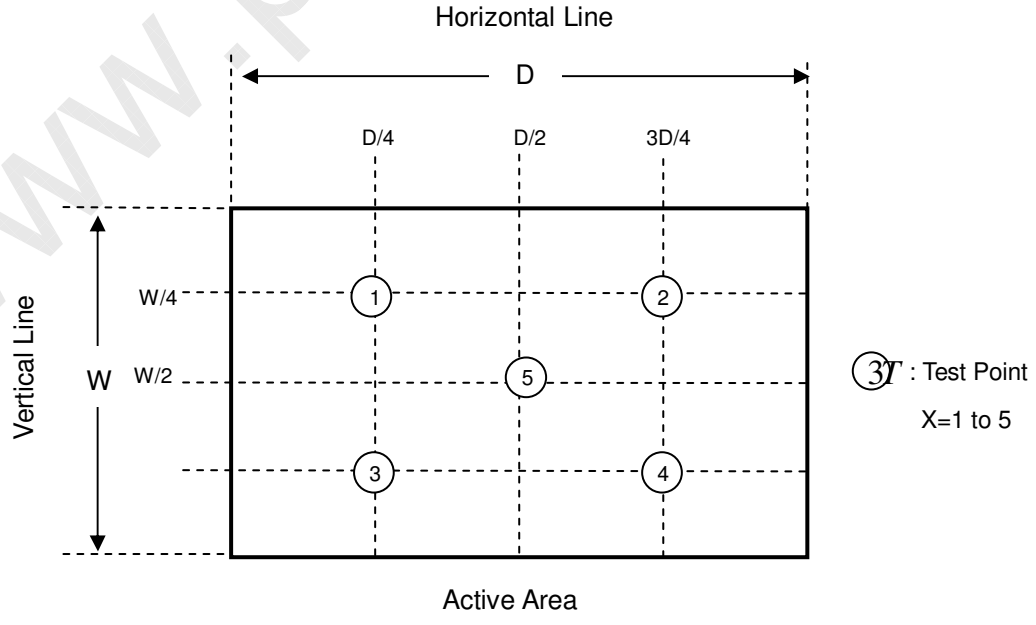
Y_B = Luminance of measured location with gray level 255 pattern (cd/m2)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMIS LSI chips.

[5] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.

[6] Do not plug in or pull out the I/F connector while the module is in operation.

[7] Do not disassemble the module.

[8] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[9] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[10] When storing modules as spares for a long time, the following precaution is necessary.

[10.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity without condensation.

[10.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[11] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

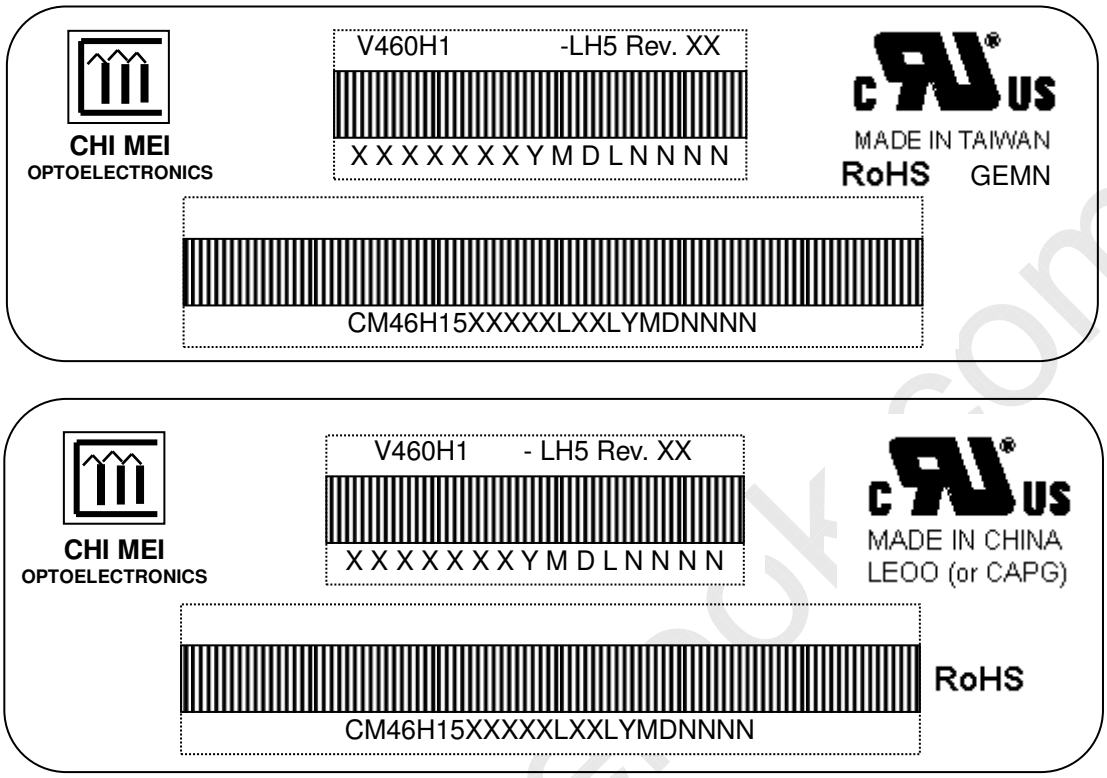
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V460H1-LH5

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X-XX	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…. Month: 1~9, A~C for Jan. ~ Dec. Day: 1~9, A~Y for 1st to 31st , exclude I, O, and U
L	Product line #	1→ Line 1, 2→ Line 2,…etc.
NNNN	Serial number	Manufacturing sequence of product

(d) Customer's barcode definition:

Serial ID: CM-46H15-X-X-X-XX-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMI=CM
46H11	Model number	V460H1-LH5=46H15
X	Revision code	C1=A, C2=B, ...
X	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatek=C, OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
X	Gate driver IC code	
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	1~12=0~C
XX	Module location	Tainan, Taiwan=TN
L	Module line #	1~12=0~C
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…. Month: 1~9, A~C for Jan. ~ Dec. Day: 1~9, A~Y for 1st to 31st , exclude I, O, and U
NNNN	Serial number	By LCD supplier

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 3 LCD TV modules / 1 Box

(2) Box dimensions : 1190(L)x280(W)x712(H)mm

(3) Weight : Approx. 46Kg (3 modules per carton)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

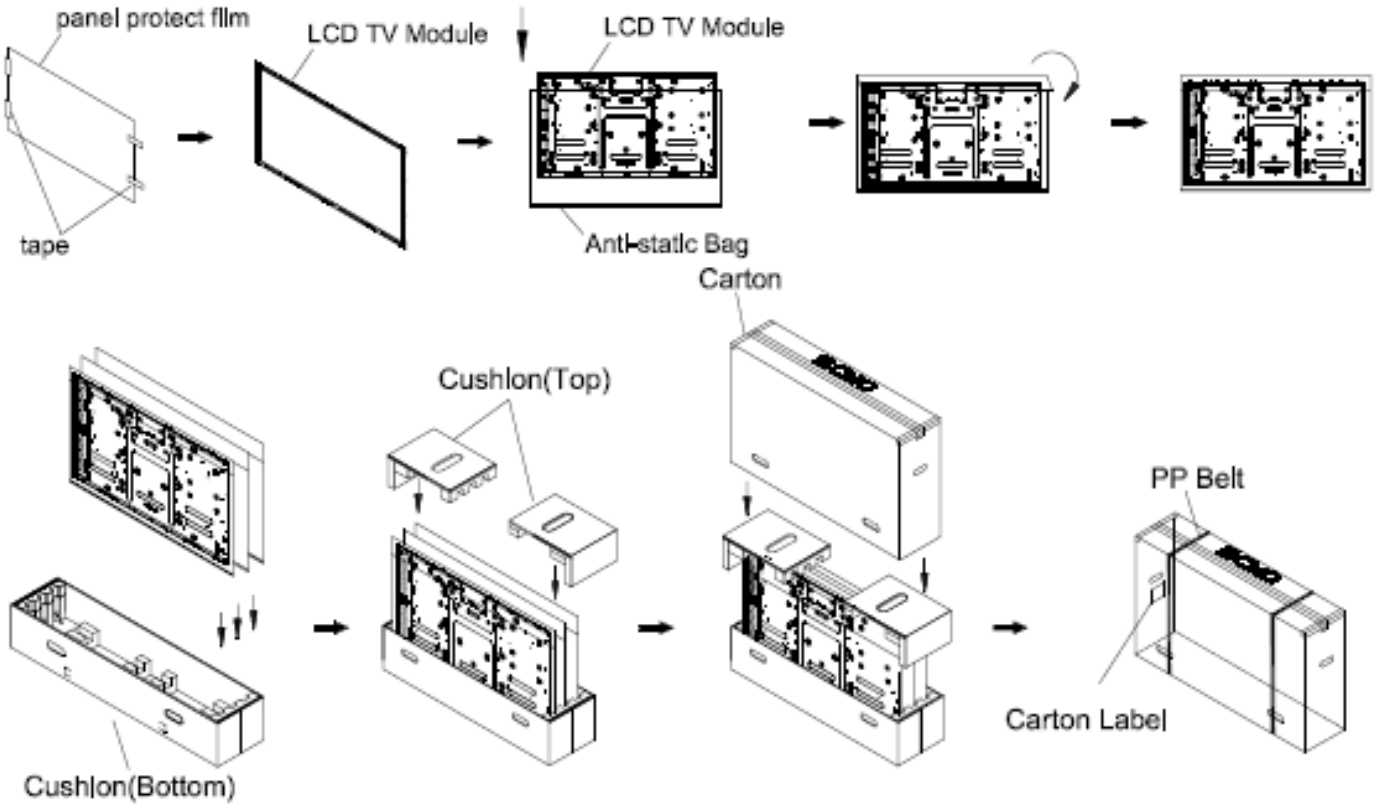


Figure 10-1 packing method

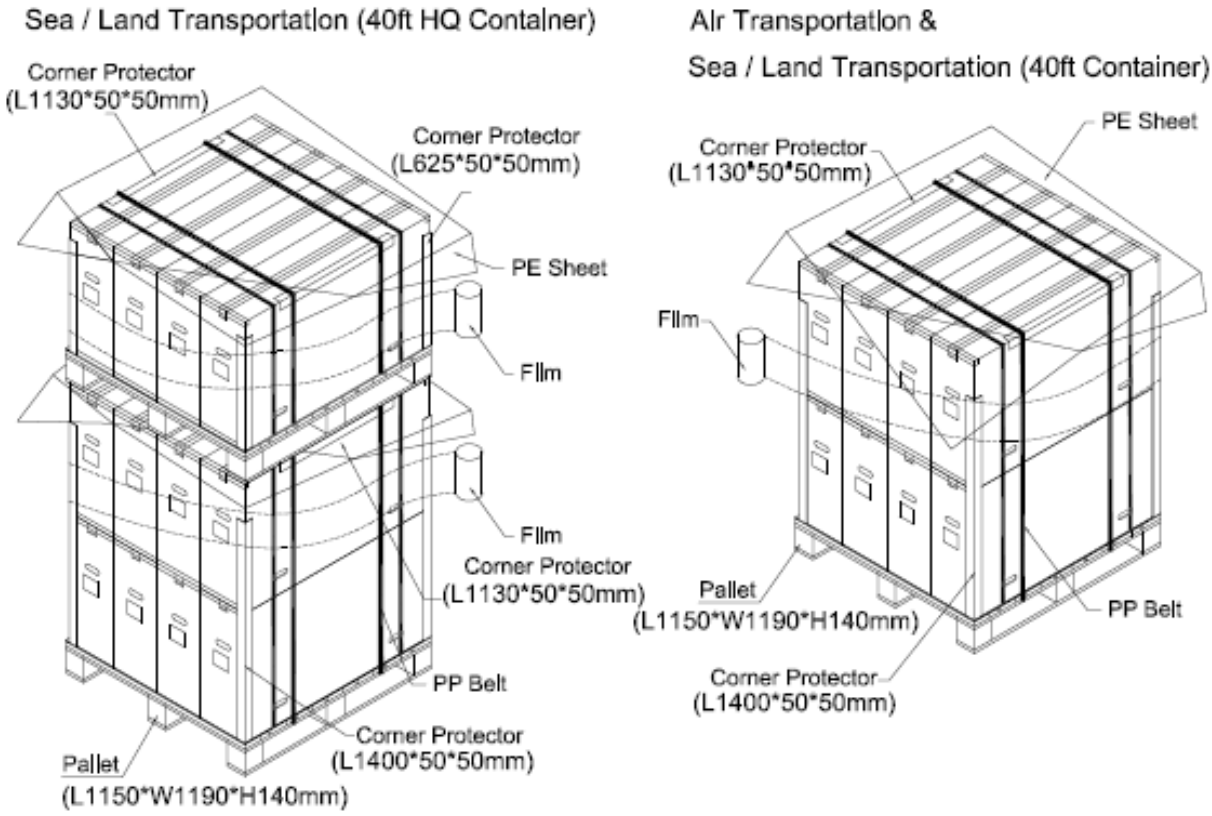


Figure 10-2 packing method

11. MECHANICAL CHARACTERISTIC